Davis Ranney

PHD CANDIDATE | COMPUTER ENGINEERING – HARDWARE SECURITY

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Research

VortexShield: Protecting RISC-V GPU Caches from Fine-Grained Attacks
Davis Ranney, Andrew Jacob, Amir Taherin, A. Adam Ding, David Kaeli, Yunsi Fei *Active Project*

- Designing a secure cache architecture for the open-source RISC-V Vortex GPU to be resistant against cache attacks
- Executing an AES key recovery attack on Vortex and assessing various secure cache designs for attack mitigation, and measuring the performance overhead of each for several GPU workloads

Exploring the Limits of Side-Channel Protections in ML-KEM Verification Hardware Implementations
Davis Ranney, Yashaswini I Makaram, A. Adam Ding, Yunsi Fei *Pending Publication*

- Identified specific difficulties of securing hardware-accelerated ML-KEM against EM and power side-channel attacks by implementing proposed protections and cutting-edge attack methodologies
- Evaluated multiple levels of masking and protections and validated an over 90% attack success rate on FPGAs and microcontrollers across previously proposed mitigations, reinforcing the need for better protections

USBSnoop: Revealing Device Activities via USB Congestions
Davis Ranney, Yufei Wang, A. Adam Ding, Yunsi Fei *HOST 2025*

- Pioneered a novel USB side-channel attack leveraging congestion of multiple USB devices across a USB Hub to profile devices and extract sensitive information, compromising user privacy and security
- Demonstrated a keystroke recovery attack with a mouse and keyboard with over 80% accuracy, and a web traffic recovery attack with a mass storage device and an Ethernet adapter with over 94% accuracy

Experience

Hardware Verification Engineer Co-op | *Apple, Inc*. **March 2021 – September 2021**

- Developed data processing tools and data visualization tools to evaluate hundreds of M-Series MacBook prototypes and identify problematic tests, components, and devices while also isolating outliers and quickly interpreting patterns that needed further inspection or escalation
- Optimized test sequences to thoroughly and efficiently execute across multiple hardware configurations and generations, reducing several tests to execute in minutes rather than hours

FPGA/ASIC Engineering Co-op | *L3Harris Technologies* **March 2020 – September 2020**

- Implemented and validated custom FPGA cores to run symmetric key encryption algorithms for high-speed SSD storage devices with a throughput of over 1 gigabyte per second
- Leveraged Vivado HLS to quickly design cores in C++ and Mentor Questa to ensure functionality and performance while researching NVMe and AXI protocols to optimize design integration

Education

Northeastern University - PhD in Computer Engineering **2022-2027**

Drexel University - MS in Computer Science | BS in Computer Engineering **2017-2022**

Technical Skills

Python, C Programming, Java, C++, Git, Javascript
Verilog, VHDL, SQL, Bash, AWK, Make
Secret Level Security Clearance
Xilinx Vivado, Mentor Questa, ModelSim
Autodesk Fusion 360
Adobe Photoshop, Premiere Pro, After Effects